What is claimed is:

1. A semiconductor integrated circuit comprising:

an internal supply voltage generation circuit which generates an internal supply voltage by decreasing an external supply voltage; and

an internal circuit which operates with the internal supply voltage supplied thereto,

wherein the internal supply voltage generation circuit changes the internal supply voltage level to be generated in accordance with an operation speed of the internal circuit.

2. The semiconductor integrated circuit according to claim 1 further comprising:

a clock control circuit which generates an internal clock signal having a frequency controlled in accordance with the operation speed of the internal circuit,

wherein, when the internal clock signal is controlled to have a first frequency, the internal supply voltage is controlled to have a first voltage, and when the internal clock signal is controlled to have a second frequency which is lower than the first frequency, the internal supply voltage is controlled to have a second voltage which is lower than the first voltage.

3. The semiconductor integrated circuit according to claim 1 further comprising:

a clock and voltage control circuit which generates an internal clock signal having a frequency controlled in accordance with the operation speed of the internal circuit,

said clock and voltage control circuit controls the internal clock signal frequency, and also controls the internal supply voltage level generated by the internal supply voltage generation circuit to become a level corresponding to the internal clock signal frequency.

4. The semiconductor integrated circuit according to claim 3,

wherein, when the internal clock signal is controlled to have a first frequency, the internal supply voltage is controlled to have a first voltage, and when the internal clock signal is controlled to have a second frequency which is lower than the first frequency, the internal supply voltage is controlled to have a second voltage which is lower than the first voltage.

5. The semiconductor integrated circuit according to claim 2,

wherein the controlled voltage level of the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each internal clock signal frequency.

6.The semiconductor integrated circuit according to claim 3,

wherein the controlled voltage level of the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each internal clock signal frequency.

7.The semiconductor integrated circuit according to claim 4,

wherein the controlled voltage level of the internal supply voltage is set higher than the minimum voltage level, over which the internal circuit is operational at each internal clock signal frequency.

8. The semiconductor integrated circuit according to claim 2,

wherein, when the internal supply voltage is controlled to increase from the second voltage to the first voltage, the internal clock signal frequency is controlled to change from the second frequency to the first frequency after increasing the internal supply voltage generated by the internal supply voltage generation circuit to the first voltage is ascertained to complete.

9. The semiconductor integrated circuit according to claim 4,

wherein, when the internal supply voltage is

controlled to increase from the second voltage to the first voltage, the internal clock signal frequency is controlled to change from the second frequency to the first frequency after increasing the internal supply voltage generated by the internal supply voltage generation circuit to the first voltage is ascertained to complete.

10. The semiconductor integrated circuit according to claim 1,

wherein, when the internal circuit is controlled to set into standby mode, the internal supply voltage generation circuit suspends generation of the internal supply voltage.

11. The semiconductor integrated circuit according to claim 10, further comprising:

an external reset circuit which generates an initialization signal to restore the internal circuit from the standby mode,

wherein, in response to said initialization signal, the internal supply voltage generation circuit resumes generation of the internal supply voltage.

12. The semiconductor integrated circuit according to claim 1,

wherein, when turning on power, the internal supply voltage is controlled to have a maximum internal supply

voltage level.

13. The semiconductor integrated circuit according to claim 2,

wherein, in accordance with a program executed by a CPU in the internal circuit, the internal clock signal frequency generated by the clock control circuit is controlled, and further the internal supply voltage level generated by the internal supply voltage generation circuit is controlled.

14. The semiconductor integrated circuit according to claim 13,

wherein the executed program determines an operation is performed in either a high-speed operation mode or a low-speed operation mode, and when determined as being in the high-speed operation mode, the internal clock signal frequency is controlled to be higher, and also the internal supply voltage is controlled to be higher, while when in the low-speed operation mode, the internal clock signal frequency is controlled to be lower, and also the inter supply voltage is controlled to be lower.

15. The semiconductor integrated circuit according to claim 13 further comprising:

a first register which supplies a voltage control signal to the internal supply voltage generation circuit;

and

a second register which supplies an operation mode signal to the clock control circuit,

wherein the CPU modifies data stored in at least either one of the first register and the second register, depending on the executed program.